Accelerate Your Time-to-Mission™

Discrete I/O SF
DT2
Function Module

MODULE MANUAL

Revision History

Revision	Revision Date	Description	Author
A	2/1/2018	Initial release	SL
A1	2/13/2018	ECO C05364, update to title page	SL
A2	3/5/2018	ECO C05412, updates to module manual consistency	SL
A3	12/18/2018	ECO C06056, typo correction in specifications section.	SL

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Introduction

This module manual provides information about the North Atlantic Industries, Inc. (NAI) Discrete Function Module: DT2. This module is compatible with all NAI Generation 5 motherboards.

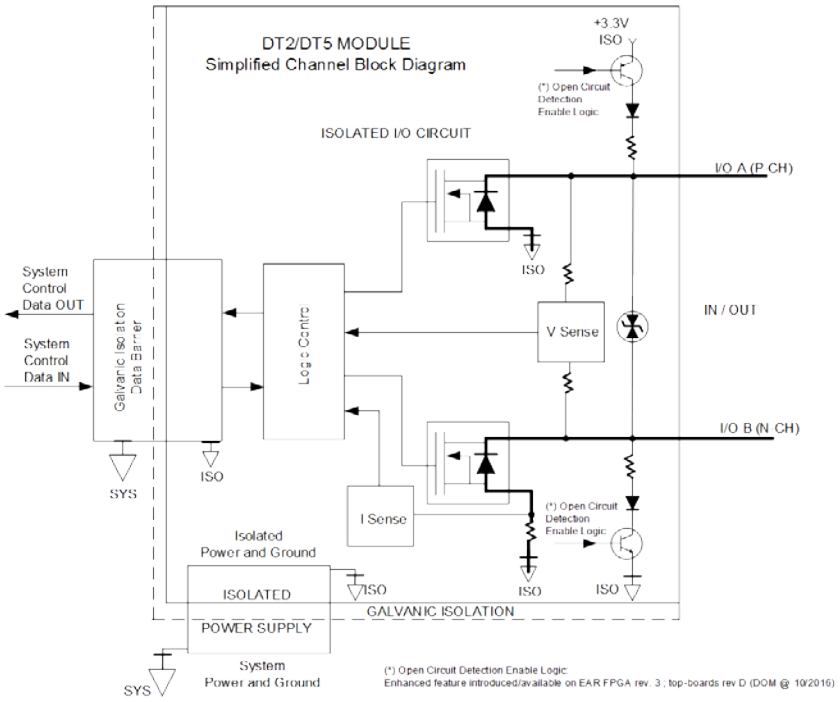
The DT2 Discrete module is a digital I/O 32-Bit module that provides 16 individual channels that either can be used for input voltage measurements, or as a bidirectional current switch.

Features

- 16 channels available as inputs or outputs
- Programmable for Input voltage or switch closure for each channel
- Continuous background built-in-test (BIT) (during normal operation, status provided for channel health and operation feedback)
- Ability to read switch I/O voltage and current
- Ability to handle switch closure currents of up to 625ma DC
- Automatic switch overcurrent protection, programmable to 625 mA max
- Open Circuit Detection
- Supports ‘dual turn-on’ (series channel output) applications (e.g. dual series ‘key’ missile launch control)
- Clean, bounce-free switching

Specifications

Discrete I/O - 16-Channel SF Module DT2



INPUT CHARACTERISTICS

Input Range:	±80 V (peak) / ±60 V (typical)
Input Pulse Detection:	A pulse of 40 µs min. width will be sensed and indicated by the appropriate Hi–Lo or Lo-Hi Transition Interrupt.
Input Impedance:	2 MΩ / (200 kΩ if/when Open Circuit Detect Logic enabled)
Switching Threshold:	Levels are programmable from 0 to 80 Vrms with 10-bit resolution (0.98% FS) On/Off.
Accuracy of Set Point:	The greater of 5% signal value or 0.25 V.
ON/OFF Differential	0.5 V min. recommended.
Debounce:	Programmable per channel from 0 to 10 µs x 2^{32} (LSB= 10 µs; 32-bit resolution). (pending characterization)
Update Rate:	Each channel is updated every 10 µs.
Overvoltage Protection:	Input clamped at ±80 VDC.
Voltage Measurement:	User can read input voltage of each channel. From: LSB=100mV; Accuracy: ±3 LSB's (300 mV) over temp. To: 1% FSR

SWITCH CHARACTERISTICS

Switch Formats:	Isolated bidirectional (AC/DC) MOSFET switch.
Switch Current:	0-625 mA per channel (load determined) / (±80 V peak)
Switch Impedance Open:	2 MΩ / (200 kΩ if/when Open Circuit Detect Logic enabled)
Switch Impedance Closed:	0.5 Ω typical, 1 Ω max.
Current Measurement:	User can read AC/DC current through switch, independently for each channel, LSB=3 mA; Accuracy: The greater of ±10% of Signal or ±20 mA over temperature.
Measurement Update Rate:	Each channel is updated every 10 µs.
Isolation:	500 V (between channels and each channel to system GND).
Power:	5 VDC/0.98 A max.
Weight:	1.5 oz. (42 g)

Specifications are subject to change without notice.

Principle of Operation

DT2 provides 16 independent, isolated, programmable channels that either can be used for input voltage measurements (+/-60 V), or as a bi-directional current switch (up to 625 mA per channel). With the switch closed, both the current through the switch and the voltage across the switch can be monitored. These modules include diode clamping on each channel. Clamping is useful for inductive loads, such as relays and short circuit protection.

All 16 channels are galvanically isolated from each other and from system ground. Each channel's two-wire connection can function as an isolated voltage input or as an isolated bi-directional switch. When programmed to function as a bi-directional switch, a channel can control valves mechanical relays, indicators, etc. without concern about grounding. This module provides an automatic background built-in-test (BIT) for each channel. The BIT functions are always enabled and continually check that each channel is functioning properly.

Standard input operation is used for voltage sensing and measures both AC and DC input voltages. When operating as a switch, measurements for both voltage across and current through the switch closure are available. Current and Voltage measurements are available as both instantaneous and averaged (RMS).

Four input voltage threshold levels (Max High, Upper, Lower, Min Low) are programmed to user defined high and low voltage levels. All four of the threshold levels must be set for each Input or Output channel. Threshold crossing may be programmed to generated interrupts on a change of state.

The module design utilizes state of the art galvanic isolation that is superior to alternatives such as optocoupler devices. The galvanic isolation eliminates typical optocoupler design concerns such as uncertain current transfer ratios, nonlinear transfer functions and temperature/lifetime degradation effects.

Continuous Background Built-In Test (BIT)

BIT is always enabled, and continually checks the health of each channel. This is accomplished by internal test circuitry that is incorporated into each 16-channel module. The test circuit is sequentially connected across each channel and checks that the commanded mode (input or switch closure) is correctly set, and depending upon the configuration, verifies that the channel data agrees with the test data or a possible fault is detected. Additionally, each output is continually checked for overcurrent, which is manually set for each channel. If the switch is open and current is any value other than 0 A, a BIT error will occur. If the switch is closed and voltage is any value other than 0 V, a BIT error will occur.

Input/Switch Interface

Each channel contains a both an isolated differential amplifier and a dual N-Channel MOSFET, configured as isolated Solid-State Relay (SSR). The SSR is energized, so both AC and DC current can flow through the channels I/O pins. The MOSFET presents a low ~.5 Ω on impedance. The module contains circuitry to measure the current through the SSR and the voltage present on the I/O pins.

Register Descriptions

The register descriptions provide the register name, Register Offset, Type, Data Range, Read or Write information, Initialized Value, a description of the function and, in most cases, a data table.

Read I/O

Function: Reads High **1** or Low **0** inputs or outputs as defined by internal channel threshold values. Bit-mapped per channel.

Type: binary word (32-bit)

Read/Write: R

Initialized Value: N/A

Operational Settings: N/A

Read I/O																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Switch Control

Function: Opens and closes the switch for each channel.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0x0000 0000

Operational Settings: Write integer **0** for input; Write **1**, for closed switch.

Switch Control																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Open Circuit Detection

Function: Enables a 3.3v pull-up on the channel that may be used for open circuit detection.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0x0000 0000

Operational Settings: Write integer **1** for open circuit detection. Default is **0**, which does not provide open circuit detection. When an open circuit occurs, the voltage read on the channel will be pulled up to ~2.7 V. Normal reading is 0.

An interrupt is generated for open circuit indication, by channel, via the *Maximum High Threshold* and *Maximum High Threshold Interrupt Enable* registers.

Open Circuit Detection																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Switch State

Function: Reads whether the state of the switch is open or closed.

Type: binary word (32-bit)

Read/Write: R

Initialized Value: N/A

Operational Settings: N/A

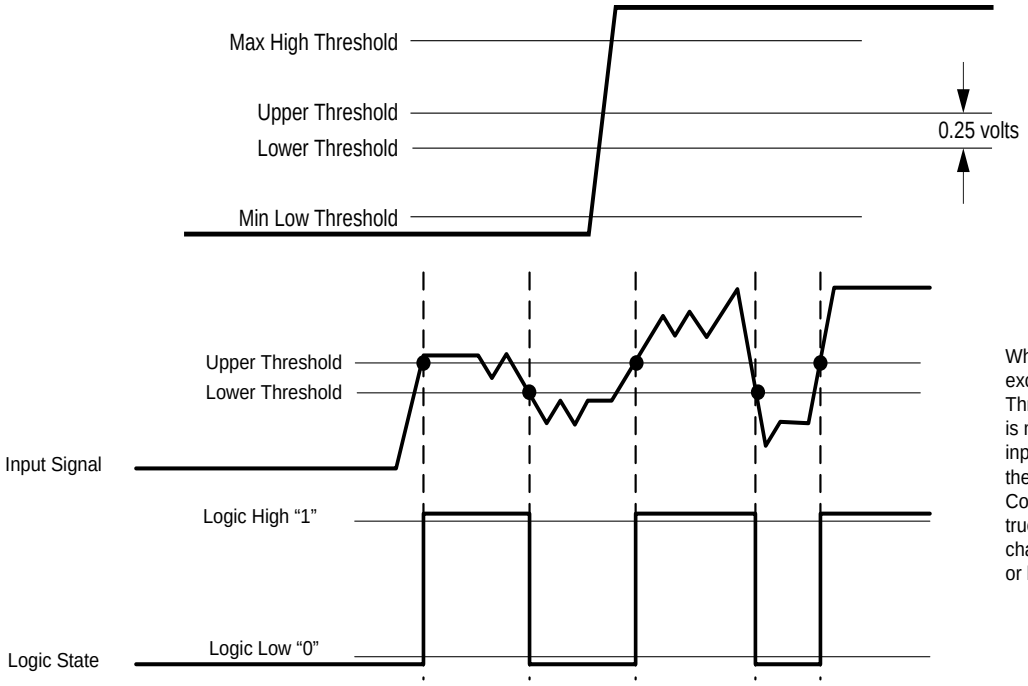
Switch State																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Threshold Programming

Four threshold levels: Max High, Upper, Lower, Min Low offer maximum user flexibility. All four threshold levels must be programmed. For input or output, the threshold levels will define the logic states. For proper operation, the threshold values should be programmed such that:

Max High Threshold > Upper Threshold > Lower Threshold > Min Low Threshold

Program Upper and Lower Thresholds, keeping the 0.25 V min. differential in mind, and then add debounce time as required. When the input signal exceeds the Upper Threshold, a logic high **1** is maintained until the input signal falls below the Lower Threshold. Conversely, when the input signal falls below the Lower Threshold, a logic low **0** is maintained until the input signal rises above the Upper Threshold.



When the input signal exceeds the Upper Threshold, a logic high "1" is maintained until the input signal falls below the Lower Threshold. Conversely, the same is true as the signal changes from low to high, or high to low.

Maximum High Threshold

Function: Sets the maximum high threshold value. Programmable per channel from -60 to +60 Vrms, with binary 10-bit word resolution (LSB=100 mv).

Type: binary word (32-bit)

Data Range: 0xFFFF FDA8 to 0x0000 0258 (usable range)

Read/Write: R/W

Initialized Value: 0x64

Operational Settings: Assumes that the programmed level is the minimum voltage used to indicate a Max. High Threshold. If a signal is greater than the Maximum High Threshold value, a flag is set in the *Maximum High Threshold* register. The *Maximum High Threshold* register may be used to monitor any type of high signal voltage condition or threshold such as a "Short to +V" as it applies to input measurement as well as contact sensing applications.

Maximum High Threshold																
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Upper Threshold

Function: Sets the upper threshold value. Programmable per channel from -60 to +60 Vrms, with binary 10-bit word resolution (LSB=100 mv).

Type: binary word (32-bit)

Data Range: 0xFFFF FDA8 to 0x0000 0258 (usable range)

Read/Write: R/W

Initialized Value: 0x32

Operational Settings: A signal is considered logic High (**1**) when its value exceeds the Upper threshold and does not consequently fall below the Lower threshold in less than the programmed Debounce time.

Upper Threshold																
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Lower Threshold

Function: Sets the lower threshold value. Programmable per channel from -60 to +60 Vrms, with binary 10-bit word resolution (LSB=163 mv).

Type: binary word (32-bit)

Data Range: 0xFFFF FDA8 to 0x0000 0258 (usable range)

Read/Write: R/W

Initialized Value: 0x1E

Operational Settings: A signal is considered logic Low (**0**) when its value falls below the Lower threshold and does not consequently rise above the Upper Threshold in less than the programmed Debounce time.

Lower Threshold																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Minimum Low Threshold

Function: Sets the minimum low threshold. Programmable per channel from -60 to +60 Vrms, with binary 10-bit word resolution (LSB=100 mv).

Type: binary word (32-bit)

Data Range: 0xFFFF FDA8 to 0x0000 0258 (usable range)

Read/Write: R/W

Initialized Value: 0x0

Operational Settings: Assumes that the programmed level is the maximum voltage used to indicate a minimum low threshold. If a signal is less than the Min Low Threshold value, a flag is set in the *Minimum Low Threshold Status* register. The *Minimum Low Threshold* register may be used to monitor any type of low signal voltage condition or threshold such as a “Short to Ground” as it applies to input measurement as well as contact sensing applications.

Minimum Low Threshold																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Debounce Time

Function: Sets the Debounce time (LSB= 10 µs; 32-bit resolution) for each channel.

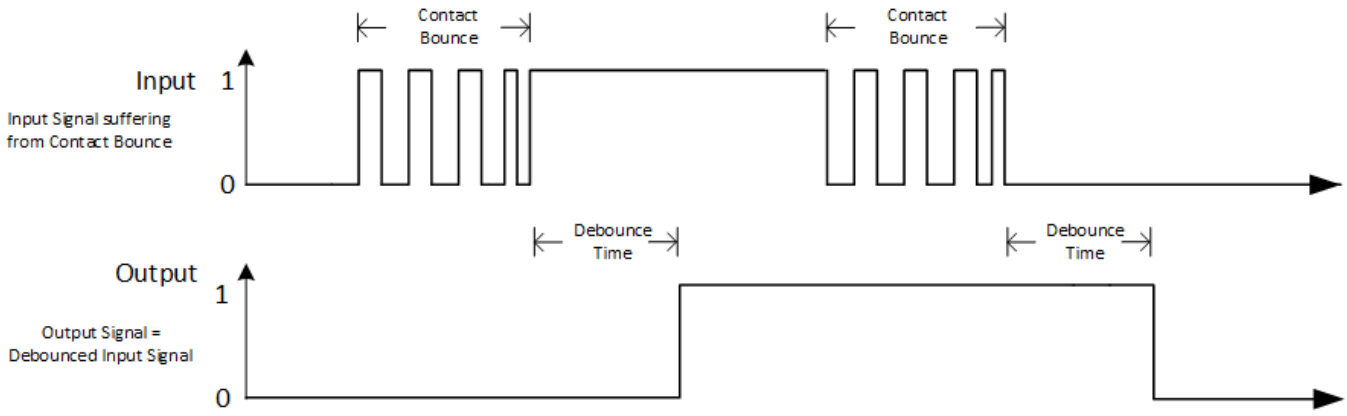
Type: binary word (32-bit)

Data Range: 0x0000 0000 to 0xFFFF FFFF

Read/Write: R/W

Initialized Value: 0

Operational Settings: The Debounce register, when programmed for a non-zero value, is used with channels programmed as input to “filter” or “ignore” expected application spurious initial transitions. Enter required debounce time into appropriate channel registers. LSB weight is 10 µs/bit (register may be programmed from 0x00000000 (debounce filter inactive) through a maximum of 0xFFFFFFFF (2^32 * 10µs). (full scale w/ 10 µs resolution). Once a signal level is a logic voltage level period longer than the debounce time (Logic High and Logic Low), a logic transition is validated. Signal pulse widths less than programmed debounce time are filtered. Once valid, the transition status register flag is set for the channel and the output logic changes state. Enter a value of 0 to disable debounce filtering. Debounce defaults to 0000h upon reset.



Voltage Reading (Sampled)

Function: Reads actual output voltage at I/O pin per individual channel.
Type: binary word (32-bit)
Data Range: 0xFFFF FDA8 to 0x0000 0258 (usable range)
Read/Write: R
Initialized Value: Updated by module as per conditions
Operational Settings: Value is a signed binary 32-bit word, where LSB = 100 mV. Data is read as 2's complement number. For example, if output voltage word is 0x00F0 (240d), actual voltage is 24.0 V.

Voltage Reading (Sampled)																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Voltage Reading (Averaged)

Function: Reads averaged RMS value of the output voltage at I/O pin per individual channel.
Type: binary word (32-bit)
Data Range: 0xFFFF FDA8 to 0x0000 0258 (usable range)
Read/Write: R
Initialized Value: Updated by module as per conditions
Operational Settings: Value is an unsigned binary 10-bit word, where LSB=100 mV. For example, if output voltage word is 0x00F0 (240d), actual voltage is 24 V.

Voltage Reading (Averaged)																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Value in Vrms (LSB=100 mV)
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
X	X	X	X	X	X	51.2	25.6	12.8	6.4	3.2	1.6	.8	.4	.2	.1	Value in Vrms (LSB=100 mV)
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Current Reading (Sampled)

Function: Reads actual current through the I/O pins at each channel.
Type: binary word (32-bit)
Data Range: 0xFFFF FEC8 to 0x0000 0138
Read/Write: R
Initialized Value: Updated by module as per conditions
Operational Settings: Value is signed binary 32-bit word, where LSB=2 mA. Read as 2's complement; Current source is positive, Current sink is negative. For example, if output current word is 0x0064 (100d), actual current is 200 mA.

Current Reading (Sampled)																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Value in mA (LSB=2 mA)
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
X	X	X	X	X	X	X	512	256	128	64	32	10	8	4	2	Value in mA (LSB=2 mA)
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Current Reading (Averaged)

Function: Reads averaged RMS current through the I/O pins at each channel.
Type: binary word (32-bit)
Data Range: 0xFFFF FEC8 to 0x0000 0138
Read/Write: R
Initialized Value: Updated by module as per conditions
Operational Settings: Value is signed binary 32-bit word, where LSB=2 mA. Read as 2's complement; Current source is positive, Current sink is negative. For example, if output current word is 0x 0064 (100d), actual current is (current source) 200 mA.

Current Reading (Averaged)																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Overcurrent Value

Function: Sets the overcurrent value for each channel.
Type: binary word (32-bit)
Data Range: 0xFFFF FEC8 to 0x0000 0138
Read/Write: R/W
Initialized Value: 0x138
Operational Settings: LSB = 2 mA

Overcurrent Value																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Status and Interrupt Registers

The registers may be set for any or all channels and will latch if a transition is detected on a channel or channels. Each channel(s) will remain latched until the channel is cleared. Multiple channels may be cleared simultaneously, if desired. Each channel bit in the register is polled for a read status. Any subsequent channel(s) transition, if detected, will propagate through to be read (rolling-latch).

Once the status register has been read, the act of writing a **1** back to the applicable status register to any specific bit (channel) location (bit mapped per channel), will "clear" the bit (set the bit to **0**) if the actual interruptible event condition has cleared. If the interruptible condition "event" is still persistent while clearing, this may retrigger the interrupt.

There is a corresponding Interrupt Enable and vector associated with each "Latched" Status. Each status type may be "polled" (at any time), or is "interruptible" when interrupts are enabled and the associated Interrupt Service Routine (ISR) vectors are programmed accordingly. When programmed for "interruptible" status, interrupts are typically generated and flagged with the programmed vector available as data. The host or single board computer (SBC) typically services the interrupt by a general or specific ISR, which reads the (typically) unique programmed vector (identifier of which status generated the interrupt), reads the associated status register to determine which channel in the status register was "flagged" and then "clears" the status register. This essentially resets the interrupt mechanism, which is now ready to be triggered by the next status register detected event "flag". "Latched Status" will trigger on either "sense on edge" or "sense on level" based on the settings of the associated Set Edge/Level Interrupt register. Sense on "edge" requires a change from low to high state to trigger the status detection, while sense on "level" is independent of the previous state. Unless otherwise specified, all status or fault indications are bit set per channel.

BIT Dynamic Status

Function: BIT Dynamic Status is set when a redundant measurement is inconsistent with the input measurement level detected.

Type: binary word (32-bit)

Read/Write: R

Initialized Value: 0

Operational Settings: 1 is read when a fault is detected. **0** indicates no fault detected.

BIT Dynamic Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

BIT Latched Status

Function: The *BIT Latched Status* register is set when a redundant measurement is inconsistent with the input measurement level detected.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: 1 is written when a fault is detected. **0** indicates no fault detected. Write a **1** to clear status.

Notes: Faults are detected (associated channel(s) bit set to **1**) within 10 ms (pending characterization).

BIT Latched Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

BIT Interrupt Enable

Function: When enabled, interrupts are generated for each channel when the *BIT Latched Status* register indicates a fault.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Write a **1** to enable interrupts. Write a **0** to disable interrupts.

BIT Interrupt Enable																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

BIT Set Edge/Level Interrupt

Function: Sets *BIT Latched Status* register to trigger on edge or level detection.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Program the desired status sensing (per channel); **0** = edge, **1** = level.

BIT Set Edge/Level Interrupt																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Overcurrent Dynamic Status

Function: Senses an overcurrent or overload condition for each channel and provides real-time status. The output channel is also immediately disabled at time of overcurrent sensed condition.

Type: binary word (32-bit)

Read/Write: R

Initialized Value: 0

Operational Settings: 1 is read when overcurrent or overload condition transition is sensed. **0** indicates normal status.

Notes: Status is indicated (associated channel(s) bit set to **1**), within 80 ms (pending characterization).

Overcurrent Dynamic Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Overcurrent Latched Status

Function: The *Overcurrent Latched Status* register is set when the channel senses an overcurrent or overload condition and provides latched status. The output channel is also immediately disabled at time of overcurrent sensed condition.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: 1 is written when overcurrent or overload condition transition is sensed. **0** indicates no status. Write a **1** to clear status.

Notes:

- Channel(s) shut down by overcurrent sensed can be reset by writing to the *Overcurrent Reset* register.

Overcurrent Latched Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Overcurrent Interrupt Enable

Function: When enabled, interrupts are generated for each channel when the *Overcurrent Latched Status* register senses an overcurrent or overload condition for any channel.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Write a **1** to enable interrupts. Write a **0** to disable interrupts.

Overcurrent Interrupt Enable																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Overcurrent Set Edge/Level Interrupt

Function: Sets *Overcurrent Latched Status* register to trigger on edge or level detection.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Program the desired status sensing (per channel); **0** = edge, **1** = level.

Overcurrent Set Edge/Level Interrupt																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Overcurrent Reset

Function: Resets disabled channels in *Overcurrent Latched Status* register following an overcurrent condition as measured by the *Current Reading (Sampled) Register* and the value set by the *Overcurrent Value* register.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: 1 is written to reset disabled channels. Processor will write a **0** back to the *Overcurrent Reset* register when reset process is complete.

Overcurrent Reset																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	24	23	22	21	20	19	18	17	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Max Hi Threshold Dynamic Status

Function: Indicates voltage signal has exceeded Maximum High Voltage level. Real-time event status.

Type: binary word (32-bit)

Read/Write: R

Initialized Value: 0

Operational Settings: Dynamic Status is set when the voltage is above the Max Hi Threshold set in the *Maximum High Threshold* register. The associated channel(s) bit is set to **1** and is non-latching.

Max Hi Threshold Dynamic Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Max Hi Threshold Latched Status

Function: The *Max Hi Threshold Latched Status* register is set when the voltage signal has exceeded Maximum High Voltage level set in the *Maximum High Threshold* register.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Status is indicated (bit is set) within 500 µs (pending characterization). Write a **1** to clear status.

Max Hi Threshold Latched Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Max Hi Threshold Interrupt Enable

Function: When enabled, interrupts are generated for each channel when the *Max Hi Threshold Latched Status* register senses that the voltage signal has exceeded Maximum High Voltage level.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Write a **1** to enable interrupts. Write a **0** to disable interrupts.

Maximum High Threshold Interrupt Enable																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Max Hi Threshold Set Edge/Level Interrupt

Function: Sets *Max Hi Threshold Latched Status* register to trigger on edge or level detection.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Program the desired status sensing (per channel); **0** = edge, **1** = level.

Maximum High Threshold Set Edge/Level Interrupt																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Min Lo Threshold Dynamic Status

Function: Indicates voltage signal has fallen below Minimum Low Voltage level. Real-time event status.

Type: binary word (32-bit)

Read/Write: R

Initialized Value: 0

Operational Settings: Dynamic Status is set when the voltage is below the value set in the *Minimum Low Threshold* register. The associated channel(s) bit is set to **1** and is non-latching.

Min Lo Threshold Dynamic Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Min Lo Threshold Latched Status

Function: The *Min Lo Threshold Latched Status* register is set when the voltage signal has fallen below Minimum Low Voltage level set in the *Minimum Low Threshold* register.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Status is indicated (bit is set) within 500 µs (pending characterization). Write a **1** to clear status.

Min Lo Threshold Latched Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Min Lo Threshold Interrupt Enable

Function: When enabled interrupts are generated for each channel when the *Below Min Lo Threshold Latched Status* register senses the voltage signal has fallen below the Minimum Low Voltage level.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Write a **1** to enable interrupts. Write a **0** to disable interrupts.

Min Lo Threshold Interrupt Enable																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Min Lo Threshold Set Edge/Level Interrupt

Function: Sets *Min Lo Threshold Latched Status* register to trigger on edge or level detection.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Program the desired status sensing (per channel); **0** = edge, **1** = level.

Min Lo Threshold Set Edge/Level Interrupt																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Mid-Range Dynamic Status

Function: Indicates voltage signal is in-between Upper and Lower thresholds. Real-time event status.

Type: binary word (32-bit)

Read/Write: R

Initialized Value: 0

Operational Settings: Dynamic Status is set when the voltage is in between the values set in the *Upper Threshold* and *Lower Threshold* registers. The associated channel(s) bit is set to **1** and is non-latching.

Mid-Range Dynamic Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Mid-Range Latched Status

Function: The *Mid-Range Latched Status* register is set when the voltage signal is in-between Upper and Lower thresholds set in the *Upper Threshold* and *Lower Threshold* registers.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Status is indicated (bit is set) within 500 µs (pending characterization). Write a **1** to clear status.

Mid-Range Latched Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Mid-Range Interrupt Enable

Function: When enabled interrupts are generated for each channel when the *Mid-Range Latched Status* register senses the voltage signal is in-between Upper and Lower thresholds.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Write a **1** to enable interrupts. Write a **0** to disable interrupts

Mid-Range Interrupt Enable																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Mid-Range Set Edge/Level Interrupt

Function: Sets *Mid-Range Latched Status* register to trigger on edge or level detection.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Program the desired status sensing (per channel); **0** = edge, **1** = level.

Mid-Range Set Edge/Level Interrupt																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	24	23	22	21	20	19	18	17	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Lo-Hi Transition Dynamic Status

Function: Senses Low to High transitions for each channel and provides real-time status.

Type: binary word (32-bit)

Read/Write: R

Initialized Value: 0

Operational Settings: **1** is read when a rising edge transition is sensed. **0** indicates no status.

Notes: Considered “momentary” during the actual event when detected. Programmable for level or edge sensing, status is indicated (associated channel(s) bit set to **1**) within 20 µs (pending characterization).

Lo-Hi Transition Dynamic Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Lo-Hi Transition Latched Status

Function: The *Lo-Hi Transition Latched Status* register is set when it senses Low to High transitions for each channel.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: **1** is written when a rising edge transition is sensed. **0** indicates no status. Write a **1** to clear status.

Notes: Programmable for level or edge sensing, status is indicated (associated channel(s) bit set to **1**) within 20 µs (pending characterization).

Lo-Hi Transition Latched Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Lo-Hi Transition Interrupt Enable

Function: When enabled, interrupts are generated for each channel when the *Lo-Hi Transition Latched Status* register senses a Low to High transition for any channel.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Write a **1** to enable interrupts. Write a **0** to disable interrupts.

Lo-Hi Transition Interrupt Enable																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Lo-Hi Transition Set Edge/Level Interrupt

Function: Sets *Lo-Hi Transition Latched Status* register to trigger on edge or level detection.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Program the desired status sensing (per channel); **0** = edge, **1** = level.

Lo-Hi Transition Set Edge/Level Interrupt																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Hi-Lo Transition Dynamic Status

Function: Senses High to Low transitions for each channel and provides real-time status.

Type: binary word (32-bit)

Read/Write: R

Initialized Value: 0

Operational Settings: 1 is read when a falling edge transition is sensed. **0** indicates no status.

Notes: Considered “momentary” during the actual event when detected. Programmable for level or edge sensing, status is indicated (associated channel(s) bit set to **1**) within 20 µs (pending characterization).

Hi-Lo Transition Dynamic Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Hi-Lo Transition Latched Status

Function: The *Hi-Lo Transition Latched Status* register is set when it senses High to Low transitions for each channel.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: **1** is written when a falling edge transition is sensed. **0** indicates no status. Write a **1** to clear status.

Notes: Programmable for level or edge sensing, status is indicated (associated channel(s) bit set to **1**) within 20 µs (pending characterization).

Hi-Lo Transition Latched Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Hi-Lo Transition Interrupt Enable

Function: When enabled, interrupts are generated for each channel when the *Hi-Lo Transition Latched Status* register senses a High to Low transition for any channel.

Type: binary word (32-bit)

Read/Write: R/W

Initialized Value: 0

Operational Settings: Write a **1** to enable interrupts. Write a **0** to disable interrupts.

Hi-Lo Transition Interrupt Enable																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Hi-Lo Transition Set Edge/Level Interrupt

Function: Sets *Hi-Lo Transition Latched Status* register to trigger on edge or level detection.
Type: binary word (32-bit)
Read/Write: R/W
Initialized Value: 0
Operational Settings: Program the desired status sensing (per channel); **0** = edge, **1** = level.

Hi-Lo Transition Set Edge/Level Interrupt																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Channel
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
16	15	16	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Function Register Map

0x1000	Switch Control	R/W
0x1004	Read I/O	R
0x1008	Reset Overcurrent	R/W
0x100C	Open Circuit Detection	R/W

0x2000	Voltage Reading (Sampled) Ch.1	R
0x2080	Voltage Reading (Sampled) Ch.2	R
0x2100	Voltage Reading (Sampled) Ch.3	R
0x2180	Voltage Reading (Sampled) Ch.4	R
0x2200	Voltage Reading (Sampled) Ch.5	R
0x2280	Voltage Reading (Sampled) Ch.6	R
0x2300	Voltage Reading (Sampled) Ch.7	R
0x2380	Voltage Reading (Sampled) Ch.8	R
0x2400	Voltage Reading (Sampled) Ch.9	R
0x2480	Voltage Reading (Sampled) Ch.10	R
0x2500	Voltage Reading (Sampled) Ch.11	R
0x2580	Voltage Reading (Sampled) Ch.12	R
0x2600	Voltage Reading (Sampled) Ch.13	R
0x2680	Voltage Reading (Sampled) Ch.14	R
0x2700	Voltage Reading (Sampled) Ch.15	R
0x2780	Voltage Reading (Sampled) Ch.16	R

0x2004	Voltage Reading (Averaged) Ch.1	R
0x2084	Voltage Reading (Averaged) Ch.2	R
0x2104	Voltage Reading (Averaged) Ch.3	R
0x2184	Voltage Reading (Averaged) Ch.4	R
0x2204	Voltage Reading (Averaged) Ch.5	R
0x2284	Voltage Reading (Averaged) Ch.6	R
0x2304	Voltage Reading (Averaged) Ch.7	R
0x2384	Voltage Reading (Averaged) Ch.8	R
0x2404	Voltage Reading (Averaged) Ch.9	R
0x2484	Voltage Reading (Averaged) Ch.10	R
0x2504	Voltage Reading (Averaged) Ch.11	R
0x2584	Voltage Reading (Averaged) Ch.12	R
0x2604	Voltage Reading (Averaged) Ch.13	R
0x2684	Voltage Reading (Averaged) Ch.14	R
0x2704	Voltage Reading (Averaged) Ch.15	R
0x2784	Voltage Reading (Averaged) Ch.16	R

0x2008	Current Reading (Sampled) Ch.1	R
0x2088	Current Reading (Sampled) Ch.2	R
0x2108	Current Reading (Sampled) Ch.3	R
0x2188	Current Reading (Sampled) Ch.4	R
0x2208	Current Reading (Sampled) Ch.5	R
0x2288	Current Reading (Sampled) Ch.6	R
0x2308	Current Reading (Sampled) Ch.7	R
0x2388	Current Reading (Sampled) Ch.8	R
0x2408	Current Reading (Sampled) Ch.9	R
0x2C88	Current Reading (Sampled) Ch.10	R
0x2508	Current Reading (Sampled) Ch.11	R
0x2588	Current Reading (Sampled) Ch.12	R
0x2608	Current Reading (Sampled) Ch.13	R
0x2688	Current Reading (Sampled) Ch.14	R
0x2708	Current Reading (Sampled) Ch.15	R
0x2788	Current Reading (Sampled) Ch.16	R

0x200C	Current Reading (Averaged) Ch.1	R
0x208C	Current Reading (Averaged) Ch.2	R
0x210C	Current Reading (Averaged) Ch.3	R
0x218C	Current Reading (Averaged) Ch.4	R
0x220C	Current Reading (Averaged) Ch.5	R
0x228C	Current Reading (Averaged) Ch.6	R
0x230C	Current Reading (Averaged) Ch.7	R
0x238C	Current Reading (Averaged) Ch.8	R
0x240C	Current Reading (Averaged) Ch.9	R
0x248C	Current Reading (Averaged) Ch.10	R
0x250C	Current Reading (Averaged) Ch.11	R
0x258C	Current Reading (Averaged) Ch.12	R
0x260C	Current Reading (Averaged) Ch.13	R
0x268C	Current Reading (Averaged) Ch.14	R
0x270C	Current Reading (Averaged) Ch.15	R
0x278C	Current Reading (Averaged) Ch.16	R

0x2010	Debounce Time Ch.1	R/W
0x2090	Debounce Time Ch.2	R/W
0x2110	Debounce Time Ch.3	R/W
0x2190	Debounce Time Ch.4	R/W
0x2210	Debounce Time Ch.5	R/W
0x2290	Debounce Time Ch.6	R/W
0x2310	Debounce Time Ch.7	R/W
0x2390	Debounce Time Ch.8	R/W
0x2410	Debounce Time Ch.9	R/W
0x2C90	Debounce Time Ch.10	R/W
0x2510	Debounce Time Ch.11	R/W
0x2590	Debounce Time Ch.12	R/W
0x2610	Debounce Time Ch.13	R/W
0x2690	Debounce Time Ch.14	R/W
0x2710	Debounce Time Ch.15	R/W
0x2790	Debounce Time Ch.16	R/W

0x2014	Max. High Threshold Ch.1	R/W
0x2094	Max. High Threshold Ch.2	R/W
0x2114	Max. High Threshold Ch.3	R/W
0x2194	Max. High Threshold Ch.4	R/W
0x2214	Max. High Threshold Ch.5	R/W
0x2294	Max. High Threshold Ch.6	R/W
0x2314	Max. High Threshold Ch.7	R/W
0x2394	Max. High Threshold Ch.8	R/W
0x2414	Max. High Threshold Ch.9	R/W
0x2494	Max. High Threshold Ch.10	R/W
0x2514	Max. High Threshold Ch.11	R/W
0x2594	Max. High Threshold Ch.12	R/W
0x2614	Max. High Threshold Ch.13	R/W
0x2694	Max. High Threshold Ch.14	R/W
0x2714	Max. High Threshold Ch.15	R/W
0x2794	Max. High Threshold Ch.16	R/W

0x2018	Upper Threshold Ch.1	R/W
0x2098	Upper Threshold Ch.2	R/W
0x2118	Upper Threshold Ch.3	R/W
0x2198	Upper Threshold Ch.4	R/W
0x2218	Upper Threshold Ch.5	R/W
0x2298	Upper Threshold Ch.6	R/W
0x2318	Upper Threshold Ch.7	R/W
0x2398	Upper Threshold Ch.8	R/W
0x2418	Upper Threshold Ch.9	R/W
0x2C98	Upper Threshold Ch.10	R/W
0x2518	Upper Threshold Ch.11	R/W
0x2598	Upper Threshold Ch.12	R/W
0x2618	Upper Threshold Ch.13	R/W
0x2698	Upper Threshold Ch.14	R/W
0x2718	Upper Threshold Ch.15	R/W
0x2798	Upper Threshold Ch.16	R/W

0x201C	Lower Threshold Ch.1	R/W
0x209C	Lower Threshold Ch.2	R/W
0x211C	Lower Threshold Ch.3	R/W
0x219C	Lower Threshold Ch.4	R/W
0x221C	Lower Threshold Ch.5	R/W
0x229C	Lower Threshold Ch.6	R/W
0x231C	Lower Threshold Ch.7	R/W
0x239C	Lower Threshold Ch.8	R/W
0x241C	Lower Threshold Ch.9	R/W
0x249C	Lower Threshold Ch.10	R/W
0x251C	Lower Threshold Ch.11	R/W
0x259C	Lower Threshold Ch.12	R/W
0x261C	Lower Threshold Ch.13	R/W
0x269C	Lower Threshold Ch.14	R/W
0x271C	Lower Threshold Ch.15	R/W
0x279C	Lower Threshold Ch.16	R/W

0x2020	Min. Low Threshold Ch.1	R/W
0x20A0	Min. Low Threshold Ch.2	R/W
0x2120	Min. Low Threshold Ch.3	R/W
0x21A0	Min. Low Threshold Ch.4	R/W
0x2220	Min. Low Threshold Ch.5	R/W
0x22A0	Min. Low Threshold Ch.6	R/W
0x2320	Min. Low Threshold Ch.7	R/W
0x23A0	Min. Low Threshold Ch.8	R/W
0x2420	Min. Low Threshold Ch.9	R/W
0x2CA0	Min. Low Threshold Ch.10	R/W
0x2520	Min. Low Threshold Ch.11	R/W
0x25A0	Min. Low Threshold Ch.12	R/W
0x2620	Min. Low Threshold Ch.13	R/W
0x26A0	Min. Low Threshold Ch.14	R/W
0x2720	Min. Low Threshold Ch.15	R/W
0x27A0	Min. Low Threshold Ch.16	R/W

0x2024	Overcurrent Value Ch.1	R/W
0x20A0	Overcurrent Value Ch.2	R/W
0x2124	Overcurrent Value Ch.3	R/W
0x21A0	Overcurrent Value Ch.4	R/W
0x2224	Overcurrent Value Ch.5	R/W
0x22A0	Overcurrent Value Ch.6	R/W
0x2324	Overcurrent Value Ch.7	R/W
0x23A0	Overcurrent Value Ch.8	R/W
0x2424	Overcurrent Value Ch.9	R/W
0x2CA0	Overcurrent Value Ch.10	R/W
0x2524	Overcurrent Value Ch.11	R/W
0x25A0	Overcurrent Value Ch.12	R/W
0x2624	Overcurrent Value Ch.13	R/W
0x26A0	Overcurrent Value Ch.14	R/W
0x2724	Overcurrent Value Ch.15	R/W
0x27A0	Overcurrent Value Ch.16	R/W

BIT

0x0800	BIT Dynamic Status	R
0x0804	BIT Latched Status	R/W
0x0808	BIT Interrupt Enable	R/W
0x080C	BIT Set Edge/Level Interrupt	R/W

Overcurrent

0x0810	Overcurrent Dynamic Status	R
0x0814	Overcurrent Latched Status	R/W
0x0818	Overcurrent Interrupt Enable	R/W
0x081C	Overcurrent Set Edge/Level Interrupt	R/W

Threshold

0x0820	Max. Hi Threshold Dynamic Status	R
0x0824	Max. Hi Threshold Latched Status	R/W
0x0828	Max. Hi Threshold Interrupt Enable	R/W
0x082C	Max. Hi Threshold Set Edge/Level Interrupt	R/W

0x0830	Min. Lo Threshold Dynamic Status	R
0x0834	Min. Lo Threshold Latched Status	R/W
0x0838	Min. Lo Threshold Interrupt Enable	R/W
0x083C	Min. Lo Threshold Set Edge/Level Interrupt	R/W

Mid-Range

0x0840	Mid-Range Dynamic Status	R
0x0844	Mid-Range Latched Status	R/W
0x0848	Mid-Range Interrupt Enable	R/W
0x084C	Mid-Range Set Edge/Level Interrupt	R/W

Transition

0x0850	Lo-Hi Transition Dynamic Status	R
0x0854	Lo-Hi Transition Latched Status	R/W
0x0858	Lo-Hi Transition Interrupt Enable	R/W
0x085C	Lo-Hi Transition Set Edge/Level Interrupt	R/W

0x0860	Hi-Lo Transition Dynamic Status	R
0x0864	Hi-Lo Transition Latched Status	R/W
0x0868	Hi-Lo Transition Interrupt Enable	R/W
0x086C	Hi-Lo Transition Set Edge/Level Interrupt	R/W

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Status and Interrupts

MODULE MANUAL

Revision History

Revision	Revision Date	Description	Author
A	6/17/2019	Initial release	GC
A1	4/22/2020	ECO C07519: Module manuals updated for formatting consistency. No technical or specification updates.	MC

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1 Status and Interrupts

Status registers indicate the detection of faults or events. The status registers can be channel bit-mapped or event bit-mapped. An example of a channel bit-mapped register is the BIT status register, and an example of an event bit-mapped register is the FIFO status register.

For those status registers that allow interrupts to be generated upon the detection of the fault or the event, there are four registers associated with each status: *Dynamic, Latched, Interrupt Enabled*, and *Set Edge/Level Interrupt*.

Dynamic Status: The *Dynamic Status* register indicates the *current* condition of the fault or the event. If the fault or the event is momentary, the contents in this register will be clear when the fault or the event goes away. The *Dynamic Status* register can be polled, however, if the fault or the event is sporadic, it is possible for the indication of the fault or the event to be missed.

Latched Status: The *Latched Status* register indicates whether the fault or the event *has occurred* and keeps the state until it is cleared by the user. Reading the *Latched Status* register is a better alternative to polling the *Dynamic Status* register because the contents of this register will not clear until the user commands to clear the specific bit(s) associated with the fault or the event in the *Latched Status* register. Once the status register has been read, the act of writing a **1** back to the applicable status register to any specific bit (channel/event) location will "clear" the bit (set the bit to **0**). When clearing the channel/event bits, it is strongly recommended to write back the same bit pattern as read from the *Latched Status* register. For example, if the channel bit-mapped *Latched Status* register contains the value 0x0000 0005, which indicates fault/event detection on channel 1 and 3, write the value 0x0000 0005 to the *Latched Status* register to clear the fault/event status for channel 1 and 3. Writing a "1" to other channels that are not set (example 0x0000 000F) may result in incorrectly "clearing" incoming faults/events for those channels (example, channel 2 and 4).

Interrupt Enable: If interrupts are preferred upon the detection of a fault or an event, enable the specific channel/event interrupt in the *Interrupt Enable* register. The bits in *Interrupt Enable* register map to the same bits in the *Latched Status* register. When a fault or event occurs, an interrupt will be fired. Subsequent interrupts will not trigger until the application acknowledges the fired interrupt by clearing the associated channel/event bit in the *Latched Status* register. If the interruptible condition is still persistent after clearing the bit, this may retrigger the interrupt depending on the *Edge/Level* setting.

Set Edge/Level Interrupt: When interrupts are enabled, the condition on retriggering the interrupt after the Latch Register is "cleared" can be specified as "edge" triggered or "level" triggered. Note, the Edge/Level Trigger also affects how the Latched Register value is adjusted after it is "cleared" (see 1.1.1).

- *Edge triggered*: An interrupt will be retriggered when the Latched Status register change from low (0) to high (1) state. Uses for edge-triggered interrupts would include transition detections (Low-to-High transitions, High-to-Low transitions) or fault detections. After "clearing" an interrupt, another interrupt will not occur until the next transition or the re-occurrence of the fault again.
- *Level triggered*: An interrupt will be generated when the Latched Status register remains at the high (1) state. Level-triggered interrupts are used to indicate that something needs attention.

1.1 Interrupt Vector and Steering

When interrupts are enabled, the interrupt vector associated with the specific interrupt can be programmed with a unique number/identifier defined by the user such that it can be utilized in the Interrupt Service Routine (ISR) to identify the type of interrupt. When an interrupt occurs, the contents of the Interrupt Vector registers is reported as part of the interrupt mechanism. In addition to specifying the interrupt vector, the interrupt can be directed ("steered") to the native bus or to the application running on the onboard ARM processor.

1.2 Interrupt Trigger Types

In most applications, limiting the number of interrupts generated is preferred as interrupts are costly, thus choosing the correct Edge/Level interrupt trigger to use is important.

Example 1: Fault detection

This example illustrates interrupt considerations when detecting a fault like an “open” on a line. When an “open” is detected, the system will receive an interrupt. If the “open” on the line is persistent and the trigger is set to “edge”, upon “clearing” the interrupt, the system will not re-generate another interrupt. If, instead, the trigger is set to “level”, upon “clearing” the interrupt, the system will re-generate another interrupt. Thus, in this case, it will be better to set the trigger type to “edge”.

Example 2: Threshold detection

This example illustrates interrupt considerations when detecting an event like reaching or exceeding the “high watermark” threshold value. In a communication device, when the number of elements received in the FIFO reaches the high-watermark threshold, an interrupt will be generated. Normally, the application would read the count of the number of elements in the FIFO and read this number of elements from the FIFO. After reading the FIFO data, the application would “clear” the interrupt. If the trigger type is set to “edge”, another interrupt will be generated only if the number of elements in FIFO goes below the “high watermark” after the “clearing” the interrupt and then fills up to reach the “high watermark” threshold value. Since receiving communication data is inherently asynchronous, it is possible that data can continue to fill the FIFO as the application is pulling data off the FIFO. If, at the time the interrupt is “cleared”, the number of elements in the FIFO is at or above the “high watermark”, no interrupts will be generated. In this case, it will be better to set the trigger type to “level”, as the purpose here is to make sure that the FIFO is serviced when the number of elements exceeds the high watermark threshold value. Thus, upon “clearing” the interrupt, if the number of elements in the FIFO is at or above the “high watermark” threshold value, another interrupt will be generated indicating that the FIFO needs to be serviced.

1.3 Dynamic and Latched Status Registers Examples

The examples in this section illustrate the differences in behavior of the Dynamic Status and Latched Status registers as well as the differences in behavior of Edge/Level Trigger when the Latched Status register is cleared.

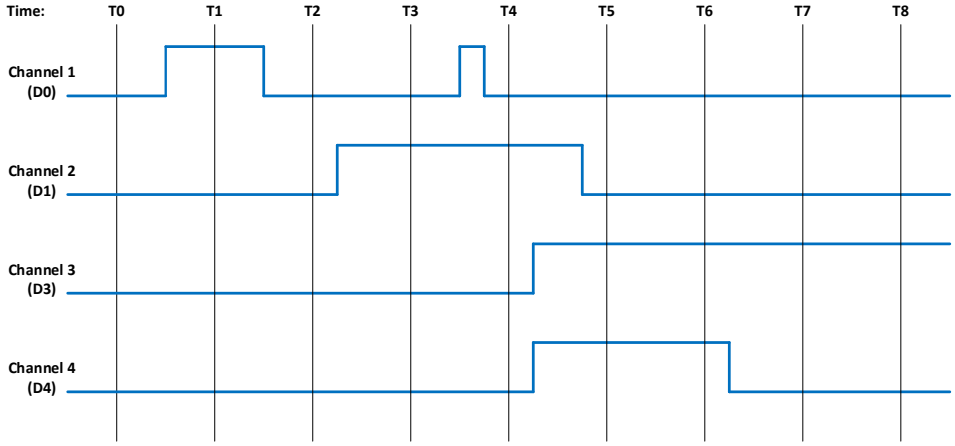

Figure 1 - Example of Module's Channel-Mapped Dynamic and Latched Status States

Time	Dynamic Status	No Clearing of Latched Status	Clearing of Latched Status (Edge-Triggered)		Clearing of Latched Status (Level-Triggered)	
		Latched Status	Action	Latched Status	Action	Latched
T0	0x0	0x0	Read Latched Register	0x0	Read Latched Register	0x0
T1	0x1	0x1	Read Latched Register	0x1		0x1
			Write 0x1 to Latched Register		Write 0x1 to Latched Register	
				0x0		*0x1*
T2	0x0	0x1	Read Latched Register	0x0	Read Latched Register	0x1
					Write 0x1 to Latched Register	
						0x0
T3	0x2	0x3	Read Latched Register	0x2	Read Latched Register	0x2
			Write 0x2 to Latched Register		Write 0x2 to Latched Register	
				0x0		*0x2*
T4	0x2	0x3	Read Latched Register	0x1	Read Latched Register	0x3
			Write 0x1 to Latched Register		Write 0x3 to Latched Register	
				0x0		*0x2*
T5	0xC	0xF	Read Latched Register	0xC	Read Latched Register	0xE
			Write 0xC to Latched Register		Write 0xE to Latched Register	
				0x0		*0xC*
T6	0xC	0xF	Read Latched Register	0x0	Read Latched Register	0xC
					Write 0xC to Latched Register	
						0xC
T7	0x4	0xF	Read Latched Register	0x0	Read Latched Register	0xC
					Write 0xC to Latched Register	
						0x4
T8	0x4	0xF	Read Latched Register	0x0	Read Latched Register	0x4

1.4 Interrupt Examples

The examples in this section illustrate the interrupt behavior with Edge/Level Trigger.

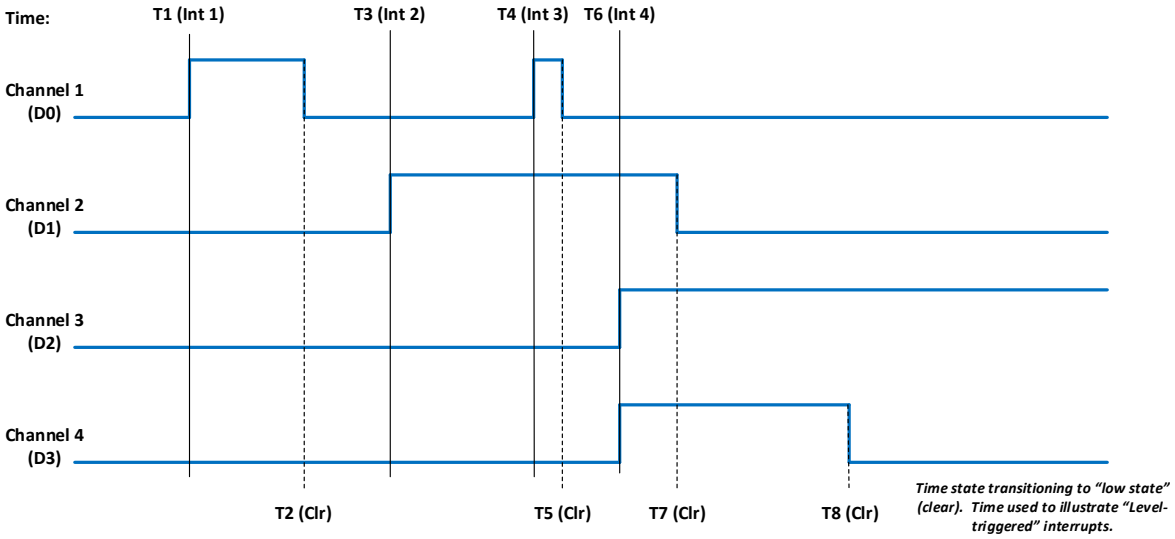

Figure 2 - Illustration of Latched Status State for Module with 4-Channels with Interrupt Enabled

Time	Latched Status (Edge-Triggered – Clear Multi-Channel) Action	Latched	Latched Status (Edge-Triggered – Clear Single Channel) Action	Latched	Latched Status (Level-Triggered – Clear Multi-Channel) Action	Latched
T1 (Int 1)	**Interrupt Generated** Read Latched Registers	0x1	**Interrupt Generated** Read Latched Registers	0x1	**Interrupt Generated** Read Latched Registers	0x1
	Write 0x1 to Latched Register		Write 0x1 to Latched Register		Write 0x1 to Latched Register	
		0x0		*0x0*	***Interrupt re-triggers*** Note, interrupt re-triggers after each clear until T2.	*0x1*
T3 (Int 2)	**Interrupt Generated** Read Latched Registers	0x2	**Interrupt Generated** Read Latched Registers	0x2	**Interrupt Generated** Read Latched Registers	0x2
	Write 0x2 to Latched Register		Write 0x2 to Latched Register		Write 0x2 to Latched Register	
		0x0		*0x0*	***Interrupt re-triggers*** Note, interrupt re-triggers after each clear until T7.	*0x2*
T4 (Int 3)	**Interrupt Generated** Read Latched Registers	0x1	**Interrupt Generated** Read Latched Registers	0x1	**Interrupt Generated** Read Latched Registers	0x3
	Write 0x1 to Latched Register		Write 0x1 to Latched Register		Write 0x3 to Latched Register	
		0x0		*0x0*	***Interrupt re-triggers*** Note, interrupt re-triggers after each clear and 0x3 is reported in Latched Register until T5.	*0x3*
					Interrupt re-triggers Note, interrupt re-triggers after each clear until T7.	*0x2*

T6 (Int 4)	**Interrupt Generated** Read Latched Registers	0xC	**Interrupt Generated** Read Latched Registers	0xC	**Interrupt Generated** Read Latched Registers	0xE
	Write 0xC to Latched Register		Write 0x4 to Latched Register		Write 0xE to Latched Register	
		0x0	***Interrupt re-triggers*** Write 0x8 to Latched Register	*0x8*	***Interrupt re-triggers*** Note, interrupt re-triggers after each clear and 0xE is reported in Latched Register until T7.	*0xE*
				0x0	***Interrupt re-triggers*** Note, interrupt re-triggers after each clear and 0xC is reported in Latched Register until T8.	*0xC*
					Interrupt re-triggers Note, interrupt re-triggers after each clear and 0x4 is reported in Latched Register always.	*0x4*

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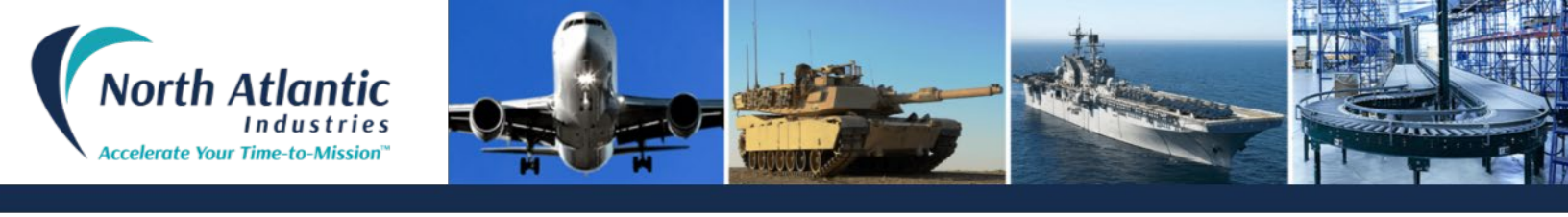

User Watchdog Timer

MODULE MANUAL
APPENDIX

Revision History

Revision	Revision Date	Description	Draft/Apprv.
A	6/25/2019	Initial release	GC
A1	10/7/2019	Appended “User” to Watchdog Timer to indicate that the Watchdog Timer is controlled by the user’s application.	GC
A2	4/22/2020	ECO C07519: Module manuals updated for formatting consistency. No technical or specification updates.	MC
B	3/29/2021	ECO C08381: Re-identified Digital-to-Synchro/Resolver (D/S) or Digital-to-L(R)VDT (D/LV) Modules are currently unsupported (at this time).	ARS

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1 User Watchdog Timer Module Manual

1.1 User Watchdog Timer Capability

The User Watchdog Timer (UWDT) Capability is available on the following modules:

- AC Reference Source Modules
  - AC1 – 1 Channel, 2-115 Vrms, 47 Hz – 20kHz
  - AC2 – 2 Channels, 2-28 Vrms, 47 Hz – 20kHz
  - AC3 – 1 Channel, 28-115 Vrms, 47 Hz – 2.5 kHz
- Differential Transceiver Modules
  - DF1/DF2 – 16 Channels Differential I/O
- Digital-to-Analog (D/A) Modules
  - DA1 – 12 Channels, ±10 VDC @ 25 mA, Voltage or Current Control Modes
  - DA2 – 16 Channels, ±10 VDC @ 10 mA
  - DA3 – 4 Channels, ±40 VDC @ ±100 mA, Voltage or Current Control Modes
  - DA4 – 4 Channels, ±80 VDC @ 10 mA
  - DA5 - 4 Channels, ±65 VDC or ±2 A, Voltage or Current Control Modes
- Digital-to-Synchro/Resolver (D/S) or Digital-to-L(R)VDT (D/LV) Modules

  (Not supported)
- Discrete I/O Modules
  - DT1/DT4 – 24 Channels, Programmable for either input or output, output up to 500 mA per channel from an applied external 3 – 60 VCC source.
  - DT2/DT5 – 16 Channels, Programmable for either input voltage measurements (±80 V) or as a bi-directional current switch (up to 500 mA per channel).
  - DT3/DT6 – 4 Channels, Programmable for either input voltage measurements (±100 V) or as a bi-directional current switch (up to 3 A per channel).
- TTL/CMOS Modules
  - TL1-TL8 – 24 Channels, Programmable for either input or output.

1.2 Principle of Operation

The User Watchdog Timer is optionally activated by the applications that require the module's outputs to be disabled as a failsafe in the event of an application failure or crash. The circuit is designed such that a specific periodic write strobe pattern must be executed by the software to maintain operation and prevent the disablement from taking place.

The User Watchdog Timer is inactive until the application sends an initial strobe by writing the value 0x55AA to the *UWDT Strobe* register. After activating the User Watchdog Timer, the application must continually strobe the timer within the intervals specified with the configurable *UWDT Quiet Time* and *UWDT Window* registers. The timing of the strobes must be consistent with the following rules:

- The application must not strobe during the Quiet time.
- The application must strobe within the Window time.
- The application must not strobe more than once in a single window time.

A violation of any of these rules will trigger a User Watchdog Timer fault and result in shutting down any isolated power supplies and/or disabling any active drive outputs, as applicable for the specific module. Upon a User Watchdog Timer event, recovery to the module shutting down will require the module to be reset.

The Figure 1 and Figure 2 provides an overview and an example with actual values for the User Watchdog Timer Strobes, Quiet Time and Window. As depicted in the diagrams, there are two processes that run in parallel. The Strobe event starts the timer for the beginning of the "Quiet Time". The timer for the Previous Strobe event continues to run to ensure that no additional Strobes are received within the "Window" associated with the Previous Strobe.

The optimal target for the user watchdog strobes should be at the interval of [Quiet time + ½ Window time] after the previous strobe, which will place the strobe in the center of the window. This affords the greatest margin of safety against unintended disablement in critical operations.

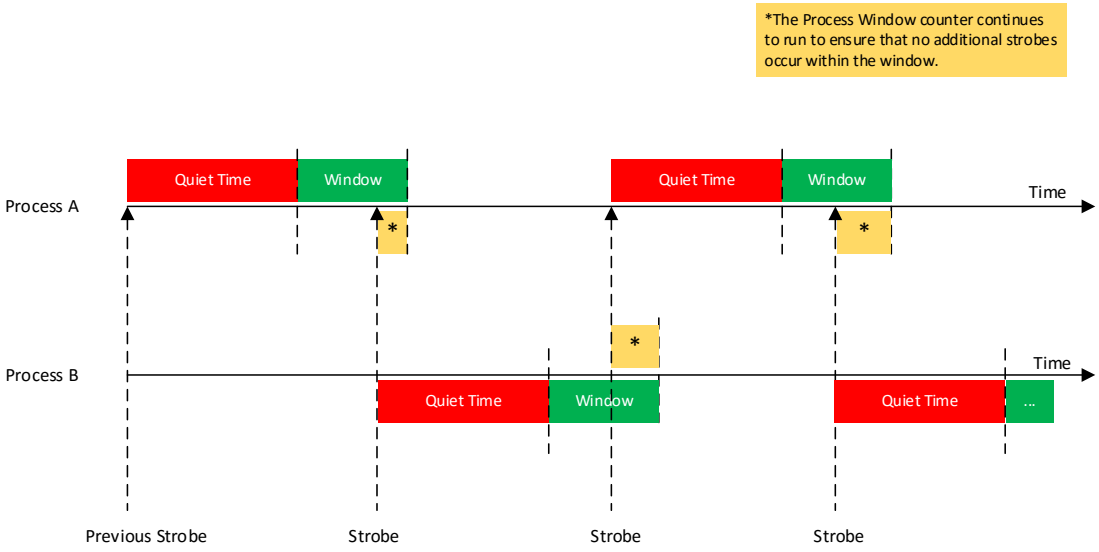

Figure 1 – User Watchdog Timer Overview

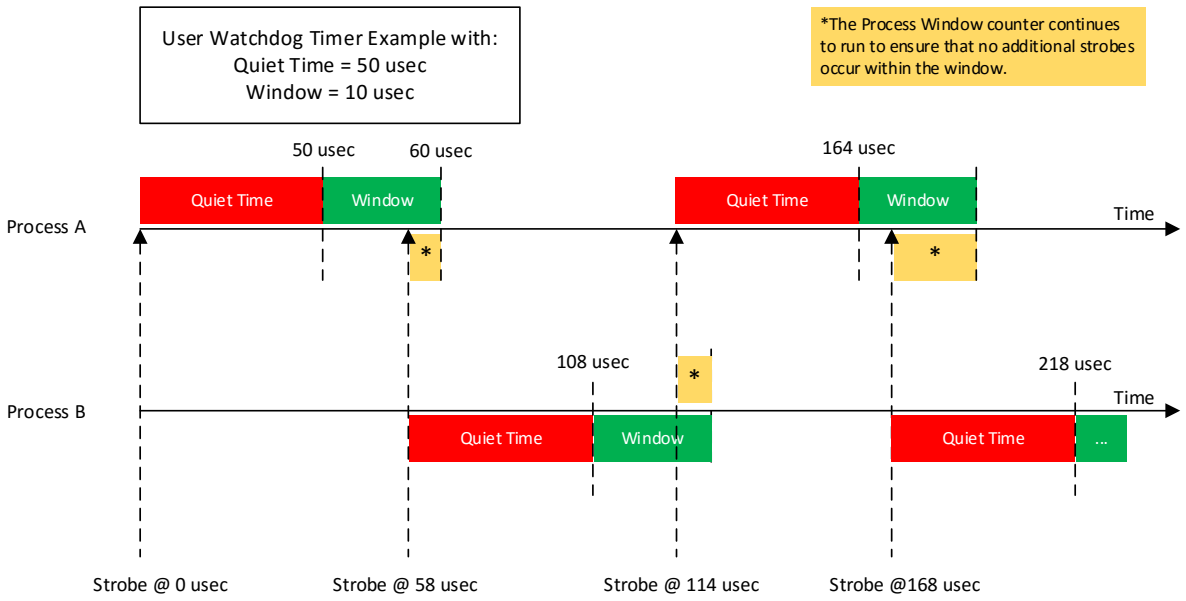

Figure 2 – User Watchdog Timer Example

Figure 3 illustrates examples of User Watchdog Timer failures.

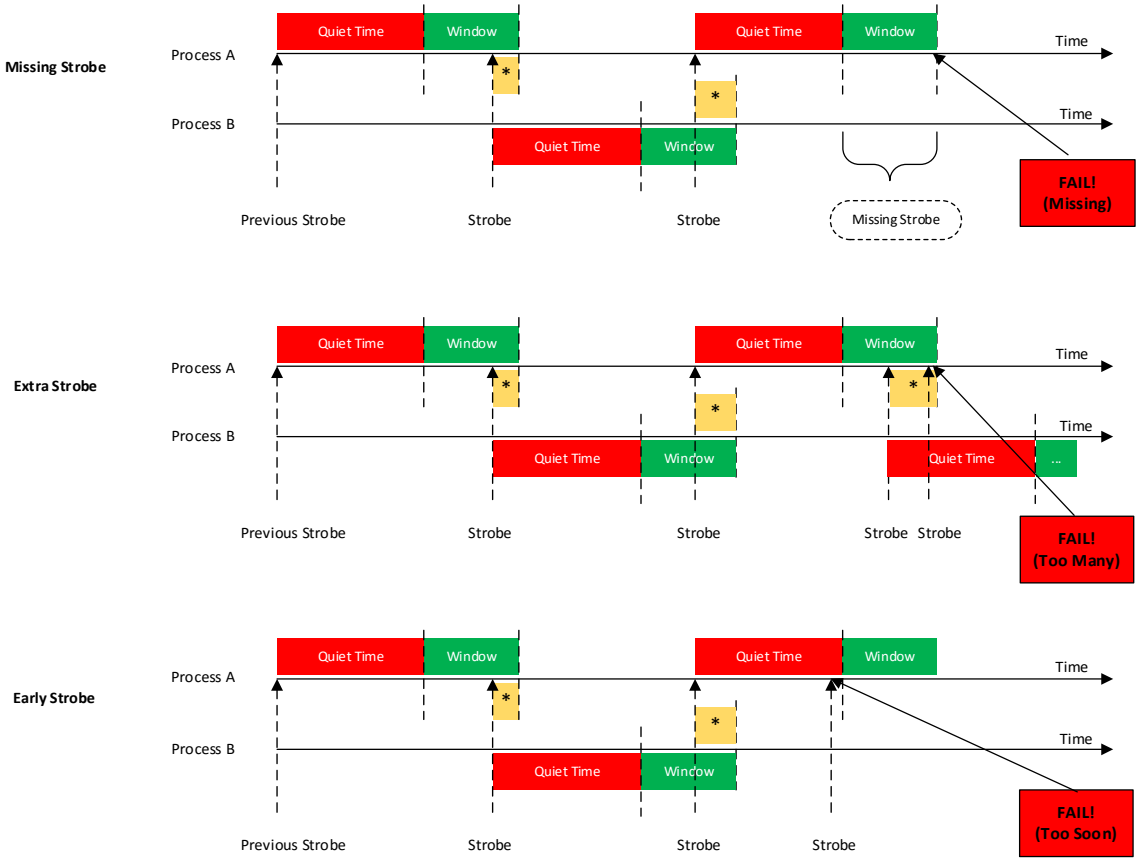

Figure 3 – User Watchdog Timer Failures

1.3 Register Descriptions

The register descriptions provide the register name, Type, Data Range, Read or Write information, Initialized Value, and a description of the function.

1.3.1 User Watchdog Timer Registers

The registers associated with the User Watchdog Timer provide the ability to specify the *UWDT Quiet Time* and the *UWDT Window* that will be monitored to ensure that EXACTLY ONE User Watchdog Timer (UWDT) Strobe is written within the window.

1.3.1.1 UWDT Quiet Time

Function: Sets Quiet Time value (in microseconds) to use for the User Watchdog Timer Frame.

Type: unsigned binary word (32-bit)

Data Range: 0 µsec to 2^32 µsec (0x0 to 0xFFFFFFFF)

Read/Write: R/W

Initialized Value: 0x0

Operational Settings: LSB = 1 µsec. The application must NOT write a strobe in the time between the previous strobe and the end of the Quiet time interval. In addition, the application must write in the *UWDT Window* EXACTLY ONCE.

1.3.1.2 UWDT Window

Function: Sets Window value (in microseconds) to use for the User Watchdog Timer Frame.

Type: unsigned binary word (32-bit)

Data Range: 0 µsec to 2^32 µsec (0x0 to 0xFFFFFFFF)

Read/Write: R/W

Initialized Value: 0x0

Operational Settings: LSB = 1 µsec. The application must write the strobe once within the Window time after the end of the Quiet time interval. The application must write in the *UWDT Window* EXACTLY ONCE.

This setting must be initialized to a non-zero value for operation and should allow sufficient tolerance for strobe timing by the application.

1.3.1.3 UWDT Strobe

Function: Writes the strobe value to be use for the User Watchdog Timer Frame.

Type: unsigned binary word (32-bit)

Data Range: 0x55AA

Read/Write: W

Initialized Value: 0x0

Operational Settings: At startup, the user watchdog is disabled. Write the value of 0x55AA to this register to start the user watchdog timer monitoring after initial power on or a reset. To prevent a disablement, the application must periodically write the strobe based on the user watchdog timer rules.

1.3.2 Status and Interrupt

The modules that are capable of User Watchdog Timer support provide status registers for the User Watchdog Timer.

1.3.2.1 User Watchdog Timer Status

The status register that contains the User Watchdog Timer Fault information is also used to indicate channel Inter-FPGA failures on modules that have communication between FPGA components. There are four registers associated with the User Watchdog Timer Fault/Inter-FPGA Failure Status: *Dynamic, Latched, Interrupt Enable,* and *Set Edge/Level Interrupt*.

User Watchdog Timer Fault/Inter-FPGA Failure Dynamic Status		
User Watchdog Timer Fault/Inter-FPGA Failure Latched Status		
User Watchdog Timer Fault/Inter-FPGA Failure Interrupt Enable		
User Watchdog Timer Fault/Inter-FPGA Failure Set Edge/Level Interrupt		
Bit(s)	**Status**	**Description**
D31	User Watchdog Timer Fault Status	**0** = No Fault **1** = User Watchdog Timer Fault
D30:D0	Reserved for Inter-FPGA Failure Status	Channel bit-mapped indicating channel inter-FPGA communication failure detection.

Function: Sets the corresponding bit (D31) associated with the channel's User Watchdog Timer Fault error.
Type: unsigned binary word (32-bit)
Data Range: 0x0000 0000 to 0xFFFF FFFF
Read/Write: R (*Dynamic*), R/W (*Latched*, *Interrupt Enable*, *Edge/Level Interrupt*)
Initialized Value: 0

1.3.2.2 Interrupt Vector and Steering

When interrupts are enabled, the interrupt vector associated with the specific interrupt can be programmed (typically with a unique number/identifier) such that it can be utilized in the Interrupt Service Routine (ISR) to identify the type of interrupt. When an interrupt occurs, the contents of the Interrupt Vector registers is reported as part of the interrupt mechanism.

In addition to specifying the interrupt vector, the interrupt can be directed ("steered") to the native bus or to the application running on the onboard ARM processor.

Note, the Interrupt Vector and Interrupt Steering registers are mapped to the Motherboard Common Memory and these registers are associated with the Module Slot position (refer to Function Register Map).

1.3.2.3 Interrupt Vector

Function: Set an identifier for the interrupt.
Type: unsigned binary word (32-bit)
Data Range: 0x0000 0000 to 0xFFFF FFFF
Read/Write: R/W
Initialized Value: 0
Operational Settings: When an interrupt occurs, this value is reported as part of the interrupt mechanism.

1.3.2.4 Interrupt Steering

Function: Sets where to direct the interrupt.
Type: unsigned binary word (32-bit)
Data Range: See table
Read/Write: R/W
Initialized Value: 0
Operational Settings: When an interrupt occurs, the interrupt is sent as specified:

Direct Interrupt to VME	1
Direct Interrupt to ARM Processor (via SerDes) *(Custom App on ARM or NAI Ethernet Listener App)*	2
Direct Interrupt to PCIe Bus	5
Direct Interrupt to cPCI Bus	6

1.3.3 Function Register Map

Key: ***Bold Italic = Configuration/Control***

Bold Underline = Status

*When an event is detected, the bit associated with the event is set in this register and will remain set until the user clears the event bit. Clearing the bit requires writing a 1 back to the specific bit that was set when read (i.e. write-1-to-clear, writing a '1' to a bit set to '1' will set the bit to '0').

1.3.3.1 User Watchdog Timer Registers

0x01C0	***UWDT Quiet Time***	R/W
0x01C4	***UWDT Window***	R/W
0x01C8	***UWDT Strobe***	W

1.3.3.2 Status Registers

User Watchdog Timer Fault/Inter-FPGA Failure

0x09B0	**Dynamic Status**	R
0x09B4	**Latched Status***	R/W
0x09B8	***Interrupt Enable***	R/W
0x09BC	***Set Edge/Level Interrupt***	R/W

1.3.3.3 Interrupt Register

The Interrupt Vector and Interrupt Steering registers are mapped to the Motherboard Memory Space and these addresses are absolute based on the module slot position. In other words, do not apply the Module Address offset to these addresses.

0x056C	***Module 1 Interrupt Vector 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x066C	***Module 1 Interrupt Steering 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x076C	***Module 2 Interrupt Vector 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x086C	***Module 2 Interrupt Steering 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x096C	***Module 3 Interrupt Vector 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x0A6C	***Module 3 Interrupt Steering 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x0B6C	***Module 4 Interrupt Vector 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x0C6C	***Module 4 Interrupt Steering 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x0D6C	***Module 5 Interrupt Vector 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x0E6C	***Module 5 Interrupt Steering 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x0F6C	***Module 6 Interrupt Vector 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W
0x106C	***Module 6 Interrupt Steering 28 – User Watchdog Timer Fault/Inter-FPGA Failure***	R/W

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